



Attorney's Docket No.: 06666-077001 / USC-3027

AP/ 2133
CFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Beerel, et al. Art Unit : 2133
Serial No. : 09/848,778 Examiner : Joseph D. Torres
Filed : May 3, 2001
Title : REDUCED-LATENCY SOFT-IN/SOFT-OUT MODULE

MAIL AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

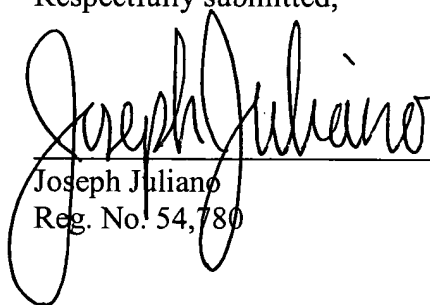
Applicants request consideration of the references listed on the attached PTO-1449 form. Under 37 C.F.R. § 1.98 (a)(2)(ii), only copies of foreign patent documents and/or non-patent literature are enclosed. Copies of any listed U.S. patents or U.S. patent application publications can be provided upon request. A copy of a communication from a foreign patent office in a counterpart application is also enclosed.

This statement is being filed within three months of the filing date of the RCE or before the receipt of a first Office Action on the merits. Please apply any charges or credits to Deposit Account No. 06 1050.

Respectfully submitted,

Date:

3/17/2005


Joseph Juliano
Reg. No. 54,780

PTO Customer No. 20985
Fish & Richardson P.C.
12390 El Camino Real
San Diego, California 92130
Telephone: (858) 678-5070
Facsimile: (858) 678-5099
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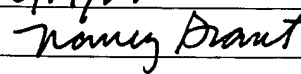
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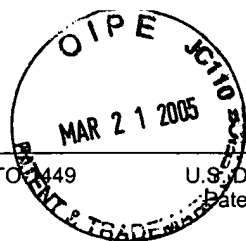
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Substitute Form PTO-1449 (Modified) Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 06666-077001	Application No. 09/848,778
	Applicant Beerel, et al.		
	Filing Date May 3, 2001	Group Art Unit 2133	

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	AD							
	AE							
	AF							

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	AG	Hsu, et al., "A Parallel Decoding Scheme for Turbo Codes", IEEE International Symposium on Circuits and Systems, March 1998, Vol. 4, pp. IV445-448
	AH	Ochi et al., "A High-Speed Decoding Method for Turbo-Code by Means of parallel Processing of Map Algorithms", Engineering Research Report of the Institute of Electronics, Information, and Communication Engineers, January 27, 1998, Vol. 97, No. 511, pp. 1-6
	AI	Brent et al., "A Regular Layout for Parallel Adders", IEEE Transactions on Computers, March 1982, Vol. C-31, No. 3, pp. 260-264
	AJ	Arjhan et al., "A Novel Scheme for Irregular Parallel-Prefix Adders", IEEE Proceedings, 12-14, 1997, pp. 74-78
	AK	Gurkaynak et al., "Higher Radix Kogge-Stone Parallel Prefix Adder Architectures", IEEE International Symposium on Circuits and Systems, May 28-31, 2000, Geneva, Switzerland, pp. V609-V612
	AL	Dimitrakopoulos et al., "High-Speed Parallel-Prefix VLSI Ling Adders", IEEE Transactions on Computers, Vol. 54, No. 2, February 2005
	AM	Janik et al., "VLSI Implementation of A 32-Bit Kozen Formulation Ladner/Fischer Parallel Prefix Adder", IEEE Proceedings, 1995, pp. 57-59
	AN	Aji et al., "The Generalized Distributive Law", IEEE Transactions on Information Theory, Vol. 46, No. 2, March 2000
	AO	Cormen, et al., "Introduction to Algorithms", published by the MIT Press under a joint production-distribution agreement with the McGraw-Hill Book Company, pp. 695-697, (1990).

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	